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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
YE, LIN	
ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,896	IKEDA ET AL.	
	Examiner	Art Unit	
	Lin Ye	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *1-4,6,7,9 and 12-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,8,10, 11 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 5, 8, 10, 11 and 15 filed on 10/18/05 have been considered but are moot in view of the new ground(s) of rejection.

Referring to claim 5, Applicant's arguments, see pages 2-5, filed on 10/18/05, with respect to the rejection(s) under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. U.S. Patent 6,044,128 in view of Date et al. U.S. Patent 5,973,558 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made under 35 U.S.C. 102(e) as being anticipated by Tomisaki et al. U.S. Patent 6,696,687.

Referring to claim 15, the response is considered necessary, since the Tanaka reference (U.S. Patent 6,044,128), will continue to be used to meet several of the claimed limitations. The claim 15 does not disclose the limitations "a correction control circuit for supplying a gate voltage with a polarity opposite to the gate voltage pulse to at least a part of the gate electrodes of the thin film transistors used for the X-ray imaging device, and the correction control circuit supplies the gate electrode with a gate voltage having a polarity of a direction that makes the mean value of the driver gate pulses at operating period be zero or reduced, during non-image reading period of the X-ray imaging device" as recited in claim 5 which teaching shift in threshold voltage can be eliminated or reduced. Therefore, the claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. U.S. Patent 6,044,128 in view of Kamimura U.S. Patent 6,081,015.

2. Since a new ground of rejection is being applied against unamended claims, this action is not made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 5 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Tomisaki et al. U.S. Patent 6,696,687.

Referring to claim 1, the Tomisaki reference discloses in Figures 4, 20A-D and 29, an X-ray imaging device comprising an X-ray-electric conversion layer (X-ray plane detector1, see Col. 3, lines 25-34), a common electrode (terminal 31a, see Col. 3, lines 48-52) arranged on one surface of the layer, a plurality of pixel electrodes (3) arranged in an array on the other surface of the layer as shown in Figure 4, a field effect thin film transistor (TFT 33, See Col. 3, lines 45-48) connected to each pixel electrode for pixel switching, including source, drain and gate electrodes, either one of source and drain electrodes being connected to the pixel electrode, the other one being connected to a signal output line (4), and the gate electrode being connected to a scanning line (5), and a field effect type thin film transistor (TFT 61, See Col. 3, lines 60-65) for imaging a signal from the field effect type thin film transistor

(TFT 33) for pixel switching, and the thin film transistor being driven by a driving gate voltage pulse (by gate drive 22) wherein the X-ray imaging device comprises a correction control circuit (adjustment block 6, see Col. 3, lines 57-68) for supplying a gate voltage with a polarity opposite to the gate voltage pulse to at least a part of the gate electrodes of the thin film transistors used for the X-ray imaging device (See Col. 4, lines 36-48), and the correction control circuit supplies the gate electrode with a gate voltage having a polarity of a direction that makes the mean value of the driver gate pulses at operating period be zero or reduced, during non-image reading period of the X-ray imaging device (See Col. 11, lines 54-67 and Col. 12, lines 1-31).

Referring to claim 10, the Tomisaki references disclose all subject matter as discussed with respected to claim 5, and the Tomisaki reference discloses in Figure 29 that the signal of the pixel electrode is picked up at every frame comprising an X-ray radiating period (by x-ay generation source 303, see Col. 13, lines 36-54) and a blanking period of non-radiating, and the non-operating period corresponds to the blanking period (e.g., the X—ray diagnoses apparatus as shown in Figure 29, the system control unit 304 supplies a control signal for synchronizing the X-ray generation sequence with the image acquisition sequence, see Col. 13, lines 55-67).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 8 and 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. U.S. Patent 6,044,128 in view of Tomisaki et al. U.S. Patent 6,696,687 and Kamimura U.S. Patent 6,081,015.

Referring to claims 5 and 8, the Tanaka reference discloses in Figures 1 and 12-14, an X-ray imaging device comprising an X-ray-electric conversion layer (X-ray plane detector 107, see Col. 3, lines 60-67), a common electrode (e.g., photo diode 148 and a pixel capacitor share a common electrode as shown in Figure 12) arranged on one surface of the layer, a plurality of pixel electrodes arranged in an array on the other surface of the layer, a field effect thin film transistor (TFT 144, See Col. 3, lines 9-10) connected to each pixel electrode for pixel switching, including source, drain and gate electrodes, either one of source and drain electrodes being connected to the pixel electrode, the other one being connected to a signal output line, and the gate electrode being connected to a scanning line (See Col. 3, lines 15-18), and a field effect type thin film transistor (TFT 146, See Col. 3, lines 20-28) for imaging a signal from the field effect type thin film transistor for pixel switching, and the thin film transistor being driven by a driving gate voltage pulse (output from horizontal scanning shift register 152 and vertical scanning shift register 150, See Col. 3, lines 20-26) wherein the X-ray imaging device comprises a correction control circuit (152 & 150) for supplying a gate voltage to the gate electrodes of the thin film transistors (e.g., the thin film transistors 144 & 146 is alternatively controlled ON-OFF by the correction control circuit 152 &150) used for the X-ray imaging device; and wherein the device comprises a protection diode (MIM Structure 9 as a protective diode, see Col. 7, lines 39-50, Col. 11, lines 37-42

and Figure s 2A-4) limiting the voltage of the pixel electrode (7) not to exceed the protection voltage, a power source (148, see Col. 3, lines 14-15 and Figure 12) supplying a predetermined voltage to the common electrode (49, see Col. 7, lines 31-33), a gate drive circuit switching the thin film transistor (TFT 5, See Col. 7, lines 25-30) by supplying a driver gate voltage pulse to the gate electrode at operating period, and a power circuit (as shown in Figure 2A) for the protection diode connected to the protection diode (9). However, the Tanaka reference does not explicitly show a detail about the correction control circuit for supplying a gate voltage with a polarity opposite to the gate voltage pulse to at least a part of the gate electrodes of the thin film transistors used for the X-ray imaging device, and the correction control circuit supplies the gate electrode with a gate voltage having a polarity of a direction that makes the mean value of the driver gate pulses at operating period be zero or reduced, during non-image reading period of the X-ray imaging device.

The Tomisaki reference discloses in Figures 4, 20A-D and 29, an X-ray imaging device comprising an X-ray-electric conversion layer (X-ray plane detector1, see Col. 3, lines 25-34), a correction control circuit (adjustment block 6, see Col. 3, lines 57-68) for supplying a gate voltage with a polarity opposite to the gate voltage pulse to at least a part of the gate electrodes of the thin film transistors used for the X-ray imaging device (See Col. 4, lines 36-48), and the correction control circuit supplies the gate electrode with a gate voltage having a polarity of a direction that makes the mean value of the driver gate pulses at operating period be zero or reduced, during non-image reading period of the X-ray imaging device (See Col. 11, lines 54-67 and Col. 12, lines 1-31). The Tomisaki reference is evidenced that one of

ordinary skill in the art at the time to see more advantages for the solid state imaging device supplying a gate voltage pulse with a polarity opposite to the gate voltage pulse to at least a part of the gate electrodes of a thin film transistors so that detecting a weak signal in e.g., fluoroscopy, since a signal can be sufficiently amplified without wasting the dynamic range and improving the S/N ratio (See Col. 6, lines 12-18). For that reason, it would have been obvious one having ordinary skill in the art at the time of the invention was made to modify the X-ray imaging device of the Tanaka ('128) by providing a gate voltage with a polarity opposite to the gate voltage pulse to at least a part of the gate electrodes of the thin film transistors used for the X-ray imaging device, and the correction control circuit supplies the gate electrode with a gate voltage having a polarity of a direction that makes the mean value of the driver gate pulses at operating period be zero or reduced, during non-image reading period of the X-ray imaging device as taught by Tomisaki ('687).

The Tanaka reference does not explicitly show the protection diode composed of a field effect type thin film transistor and the power circuit supplying a limited voltage lower than the voltage of the power source thereto, wherein the power source for the protection diode supplies a voltage lower than the limited voltage at operating period to the protection diode at non-operating period.

The Kamimura reference teaches in Figures 1A-1B, a imaging device comprising a protection diode (transistor H11, H12 and H13) are constituted of MOS thin film transistor, bipolar transistors or diodes (See Col. 55-65); and the power circuit (terminal T2 has voltage 0-5V) supplying a limited voltage (the electric strength of the gate C1, see Col. 8, lines 1-14) lower than the voltage of the power source (terminal T1 has –9V-0-15V) thereto, wherein the

power source (T1) for the protection diode (H13 and H12) supplies a voltage lower than the limited voltage at operating period to the protection diode at non-operating period (e.g., the both power circuit T2 and power source T1 supply a voltage should lower than the electric strength of the gate C1 for prevent a voltage higher than the electrical strength of the gate C1 from being destroyed, See Col. 8, lines 19-34). The Kamimura reference is evidenced that one of ordinary skill in the art at the time to see more advantages for the solid state imaging device having more flexible options to use any types transistors, diode or structures as a power protection circuit; and the power circuit supplying a limited voltage lower than the voltage of the power source thereto, wherein the power source for the protection diode supplies a voltage lower than the limited voltage at operating period to the protection diode at non-operating period, so that significantly improving a power protective function for the image device (See Col. 4, lines 45-55). For that reason, it would have been obvious one having ordinary skill in the art at the time of the invention was made to modify the X-ray imaging device of the Tanaka ('128) by providing the protection diode composed of a field effect type thin film transistor and the power circuit supplying a limited voltage lower than the voltage of the power source thereto, wherein the power source for the protection diode supplies a voltage lower than the limited voltage at operating period to the protection diode at non-operating period as taught by Kamimura ('015).

Referring to claim 11, the Tanaka, Tomisaki and Kamimura references disclose all subject matter as discussed with respected to claims 5-8, and the Tanaka reference discloses wherein the thin film transistor is made of amorphous silicon (See Col. 2, lines 25-28).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. U.S. Patent 6,044,128 in view of Kamimura U.S. Patent 6,081,015.

Referring to claim 15, the Tanaka reference discloses in Figures 1 and 12-14, an X-ray imaging device comprising an X-ray-electric conversion layer (X-ray plane detector 107, see Col. 3, lines 60-67), a plurality of pixel electrodes arranged in an array on the other surface of the layer, a field effect type thin film transistor (TFT 144, See Col. 3, lines 9-10) for pixel switching, one of whose source electrode and drain electrode is connected to the pixel electrode, the other thereof being connected to a signal output line, and whose gate electrode being connected to a scanning line (See Col. 3, lines 15-18), a protection diode (MIM Structure 9 as a protective diode, see Col. 7, lines 39-50, Col. 11, lines 37-42 and Figure s 2A-4) limiting the voltage of the pixel electrode (7) not to exceed the protection voltage, a power source (148, see Col. 3, lines 14-15 and Figure 12) supplying a predetermined voltage to the common electrode (49, see Col. 7, lines 31-33), a gate drive circuit switching the thin film transistor (TFT 5, See Col. 7, lines 25-30) by supplying a driver gate voltage pulse to the gate electrode at operating period, and a power circuit (as shown in Figure 2A) for the protection diode connected to the protection diode (9). However, the Tanaka reference does not explicitly show the protection diode composed of a field effect type thin film transistor and the power circuit supplying a limited voltage lower than the voltage of the power source thereto, wherein the power source for the protection diode supplies a voltage lower than the limited voltage at operating period to the protection diode at non-operating period.

The Kamimura reference teaches in Figures 1A-1B, a imaging device comprising a protection diode (transistor H11, H12 and H13) are constituted of MOS thin film transistor,

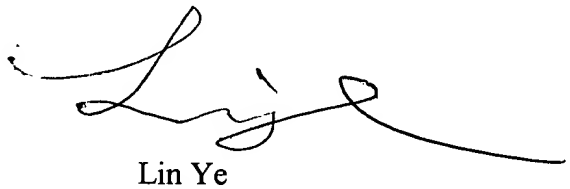
bipolar transistors or diodes (See Col. 55-65); and the power circuit (terminal T2 has voltage 0-5V) supplying a limited voltage (the electric strength of the gate C1, see Col. 8, lines 1-14) lower than the voltage of the power source (terminal T1 has –9V-0-15V) thereto, wherein the power source (T1) for the protection diode (H13 and H12) supplies a voltage lower than the limited voltage at operating period to the protection diode at non-operating period (e.g., the both power circuit T2 and power source T1 supply a voltage should lower than the electric strength of the gate C1 for prevent a voltage higher than the electrical strength of the gate C1 from being destroyed, See Col. 8, lines 19-34). The Kamimura reference is evidenced that one of ordinary skill in the art at the time to see more advantages for the solid state imaging device having more flexible options to use any types transistors, diode or structures as a power protection circuit; and the power circuit supplying a limited voltage lower than the voltage of the power source thereto, wherein the power source for the protection diode supplies a voltage lower than the limited voltage at operating period to the protection diode at non-operating period, so that significantly improving a power protective function for the image device (See Col. 4, lines 45-55). For that reason, it would have been obvious one having ordinary skill in the art at the time of the invention was made to modify the X-ray imaging device of the Tanaka ('128) by providing the protection diode composed of a field effect type thin film transistor and the power circuit supplying a limited voltage lower than the voltage of the power source thereto, wherein the power source for the protection diode supplies a voltage lower than the limited voltage at operating period to the protection diode at non-operating period as taught by Kamimura ('015).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lin Ye whose telephone number is (571) 272-7372. The examiner can normally be reached on Mon-Fri 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lin Ye
Examiner
Art Unit 2615

December 23, 2005